

WHAT IS CLAIMED IS:

1. A device including:

a Network Processor Complex Chip including a plurality of co-processors
executing programs that forward frames or hardware assist functions that performs
operations like table searches, policing and counting;

a Data Flow Chip operatively coupled to the Network Processor Complex Chip,
said Data Flow Chip including at least one port to receive/transmit data and circuit
arrangement that sets the at least one port into switch mode and/or line mode; and
a Scheduler Chip operatively coupled to the Data Flow Chip, said Scheduler Chip
scheduling frames to meet predetermined Quality of Service commitments.

2. The device of Claim 1 further including a first memory operatively coupled to the
Network Processor Complex Chip, a second memory operatively coupled to the Data
Flow Chip and a third memory operatively coupled to the Scheduler Chip.

3. A device including:

an ingress section and an egress section symmetrically arranged, said ingress
section and said egress section each including

Network Processor Complex Chip having a plurality of co-processors
programmed to execute code that forwards network traffic;

a Data Flow Chip operatively coupled to the Network Processor Complex Chip;

7 said Data Flow Chip having at least one port and circuitry to configure said port into a
8 switch mode or a line mode; and

9 a Scheduler Chip operatively coupled to said Data Flow Chip, said Scheduler
10 Chip including circuits that schedule frames to meet predetermined Quality of Service
11 commitments.

1 4. A device including:

2 an ingress section;

3 an egress section symmetrically arranged to said ingress section wherein said
4 ingress section includes a First Data Flow Chip having at least a first input port and a first
5 output port;

6 a First Network Processor Complex Chip operatively coupled to said Data Flow
7 Chip;

8 a First Scheduler Chip operatively coupled to said Data Flow Chip; and

9 said egress section including a second Data Flow Chip having at least a second
10 output and a second input;

11 a second Network Processor Chip operatively coupled to said Second Data Flow
12 Chip;

13 a second Scheduler Chip operatively coupled to the Second Data Flow Chip; and

14 communication media that wraps the Second Data Flow Chip to the First Data
15 Flow Chip.

1 5. The device of Claim 4 further including a Switch interface operatively coupled to the first
2 output port and the second input port.

1 6. The device of Claim 4 further including a line interface operatively coupled to the first
2 input port and the second output port.

1 7. A device including:

2 an ingress section; and

3 an egress section symmetrically arranged to said ingress section wherein said
4 ingress section includes a First Data Flow Chip having at least a first input port and a first
5 output port;

6 a First Network Processor Chip operatively coupled to said Data Flow Chip;

7 a First Scheduler Chip operatively coupled to said Data Flow Chip; and

8 said egress section including a second Data Flow Chip having at least a second
9 output port and a second input port;

10 a second Network Processor Chip operatively coupled to said Second Data Flow
11 Chip;

12 a second Scheduler Chip operatively coupled to the Second Data Flow Chip;

13 communication media that wraps the Second Data Flow Chip to the First Data
14 Flow Chip;

15 a first interface operatively coupled to the first output port and the second input
16 port; and
17 a second interface operatively coupling the first input port and the second output
18 port.

1 8. A network device including:
2 a switch fabric and
3 a plurality of Network Processors connected in parallel to said switch fabric
4 wherein each of the Network Processors including
5 an ingress section;
6 an egress section symmetrically arranged to said ingress section wherein said
7 ingress section including a First Data Flow Chip having at least a first input port and a
8 first output port;
9 a First Network Processor Complex Chip operatively coupled to said first Data
10 Flow Chip;
11 a First Scheduler Chip operatively coupled to said Data Flow Chip; and
12 said egress section including a second Data Flow Chip having at least a second
13 output port and a second input port;
14 a second Network Processor Chip operatively coupled to said Second Data Flow
15 Chip;
16 a second Scheduler Chip operatively coupled to the Second Data Flow Chip;

17 communication media that wraps the Second Data Flow Chip to the First Data
18 Flow Chip;
19 a first interface operatively coupled to the first output port and the second input
20 port; and
21 a second interface operatively coupling the first input port and the second output
22 port.

1 9. A Network Processor including:

2 a Network Processor Complex Chip having a plurality of co-processors;
3 a memory operatively connected to said Network Processor; and
4 a Data Flow Chip operatively coupled to said Network Processor Chip, said Data
5 Flow Chip including at least an output port, an input port; and
6 control mechanism that sets at least the input port or the output port into a switch
7 mode or a line mode.
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